a logic circuit for selectively closing and opening the gate circuit so that the sector is erased only if said sector has at least one unerased cell.

B1 Cont'd

97. A method of erasing a non-volatile electrically erasable and programmable integrated circuit memory having memory cells divided into multiple non-overlapping sectors that individually contain a plurality of said cells sufficient to store multiple bytes of data and which are erasable together, comprising:

enabling selected ones of said memory sectors to be erased;

applying an erasure pulse to the enabled sectors:

detecting for each of the selected sectors whether an unerased cell exists;

disabling those of the selected sectors which have no unerased cells; and

repeating the applying and disabling steps until all sectors are disabled.

98. The method of claim 97, wherein enabling selected sectors includes setting an erase enable latch associated with individual sectors, and wherein disabling selected sectors includes resetting the latch associated with individual sectors.

99. The method of claim 97, wherein said erasure pulse is simultaneously applied to all of said enabled sectors.--

REMARKS

The claims being added by this Amendment are either exact copies of claims 7, 13, 14, 16, 18, 19 and 21 of U.S. patent no. 5,619,451 - Costabello *et al.*, or closely patterned after them. A copy of this patent is being filed herewith.

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Respectfully submitted,

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